ERC: a trade-off between coverage and false positives?

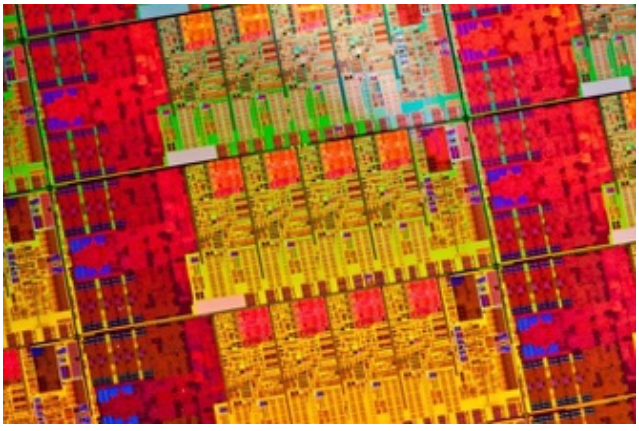
Vincent Bligny, CEO, Aniah

Electrical rule checking solutions (ERC) face a double challenge: handle the billions of transistors of a chip and be accurate enough to detect all failure modes. Any solution that does not have a good understanding of the function of each transistor and the electrical properties of each net will both miss electrical errors and falsely detect failures.

ERC has two key advantages: it reports the root cause of errors directly and unifies many design errors as a few electrical failure modes. Those advantages translate into an unparalleled effort vs. detected errors ratio.

That is, unless users must review thousands of false errors for each real one – which unfortunately is the rule more than the exception. In addition to compromising the quality of the checks, it makes ERC a tedious and complex task: false errors require an understanding of the inner workings of the analysis engine.

In this paper, we will review why the reduction of false errors is the key to both coverage and efficiency of electrical rule checking. We will further detail the causes of false errors and how they can be solved with an accurate electrical analysis engine.

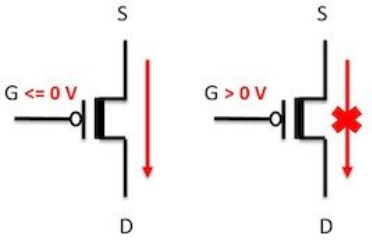


Aniah SAS
93 cours Berriat
38000 Grenoble, France
+33 4 58 00 37 74
contact@aniah.fr

1- The causes of false errors

1.1 Voltage propagation has a limited electrical accuracy

Many ERC tools rely on a technique called "voltage propagation". That means propagating values or labels from voltage supplies across devices throughout the hierarchy. Voltage drops or open devices can to some extent be accounted for, but with limitations at the IC level. The intent of this technique is to attach a set of possible voltage values for each net.



Source : allaboutcircuits.com

That technique works reasonably well for digital circuity, but it cannot account for bi-stable nets, drive strength or high impedance nets. On analog circuitry, where voltages are set by an equilibrium between several devices, that method provides limited visibility on how the circuit operates.

Another limitation of voltage propagation is its inability to choose when 2 different voltages are propagated to a single net.

Relying on this technique for ERC entails several drawbacks:

- It cannot find errors that involve any relationship between 2 or more devices without complex code development
- Non-real voltages in analog circuitry generate thousands of false errors
- Coverage on analog circuitry is limited if any
- Limited notion of electrical open (high impedance) or electrical short
- Cannot selectively search for errors specific to analog or digital

Those limitations can be illustrated on the case of common levelshifter structures:

- The levelshifter feedback structure that locks the proper state is ignored, leading to false errors
- The high-impedance errors that occur when the input stage is off cannot be identified

This case is not just theoretical: errors around level shifting are among the most common that make it to silicon undetected.

Pattern matching alleviates the limitations of voltage propagation to a certain extent but must be adapted to each variation of topology to be robust and has a strong performance impact if applied across hierarchy boundaries.

Aniah SAS
93 cours Berriat
38000 Grenoble, France
+33 4 58 00 37 74
contact@aniah.fr

1.2 Set-up errors

The power supplies being the starting point for voltage propagation, they must be set up-front - indeed, a single supply missing in the set-up may send the propagation engine into infinite loops.

With tens of supplies that can each have several values depending of the power mode, the combination of values can easily reach into the hundreds of thousands of individual cases. Choosing real scenarios is complex as supplies have interdependencies, either structurally (ex: regulated internal supplies) or because of the application constraints. Top-level supplies are known to IC integrators, but that may not be the case for internal supplies.

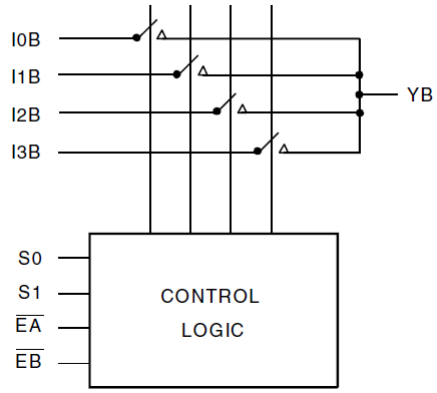
Failing to set a value for all supplies is a leading cause for false errors: the propagation engine jumps across transistors (ex: PMOS of an LDO) and assumes that the voltage downstream has the same value, which is incorrect and generates scores of false errors.

1.3 Circuit errors that are functionally impossible

Some errors are structurally correct but will not occur functionally – one may think of two mutually exclusive switches that drive a single net. The analog test structures, for example, are known to propagate "anything to anywhere" even though they will functionally set only one connected path.

Voltage propagation-based ERC cannot identify such structures that are spread across the hierarchy. The same can be said for the impact of conditional high-impedance net, that depends on what they are driving.

Here also, pattern matching can solve a part of the issue, with the limitation above-mentioned.



Source : Renesas Analog Mux / Demux

2- Mitigating the burden of false errors

2.1 Setting up a waivers flow

A commonly used technique to manage false errors is through waivers. A waiver file can be created for each IP and then used at IC level, with the promise of suppressing all false errors. This is true to some extent, but limited by:

- The analysis conditions of the IP cannot be made to match those of the IC exactly (context dependency)
- Ensuring consistency across the full IP offer is very expensive
- IPs must be analyzed with the exact same rules as the IC – new rules that may be introduced for IC-specific needs will not have waivers

Aniah SAS
93 cours Berriat
38000 Grenoble, France
+33 4 58 00 37 74
contact@aniah.fr

Narrowing the application of waivers to specific voltage conditions reduces the risk of a waiver applying outside of its scope but cannot guarantee improper waiving of real errors. Waiver also must rely on cell names, which may be a problem in case of cell re-use.

2.2 Filtering – basic and advanced

Clever, multiple-orthogonal-criteria filtering can be very effective at removing false errors. Experience, however, has proved them to be either too simple for efficiency or too complex for a wide-scale deployment of the verification solution.

The risk of filtering real errors cannot be ignored, either, and reduces filtering's capacity to eliminate false errors.

2.3 Aniah tackles the problem of false errors at its root

Aniah has been founded with one objective in mind: provide 100% coverage of electrical errors. That means that our analysis should not generate any false error. This is a cornerstone of our product.

The main means by which we remove false errors is by using an accurate electrical analysis engine that provides a reliable understanding of all topologies. Please contact us for more information on how we achieve this.

3- Conclusion: ERC benefits defined by false errors reduction

The burden of false errors offsets the elegant efficiency of ERC and, by reducing its completeness, diminishes its value. The extent to which ERC solutions are now used in the industry to detect electrical errors is largely shaped by what can be achieved while keeping false errors at bay.

In other words, a solution that would get rid of false errors would provide massive benefits to IC design engineers. Aniah was founded on this observation and its mission is to provide this game-changing solution.

Aniah SAS
93 cours Berriat
38000 Grenoble, France
+33 4 58 00 37 74
contact@aniah.fr