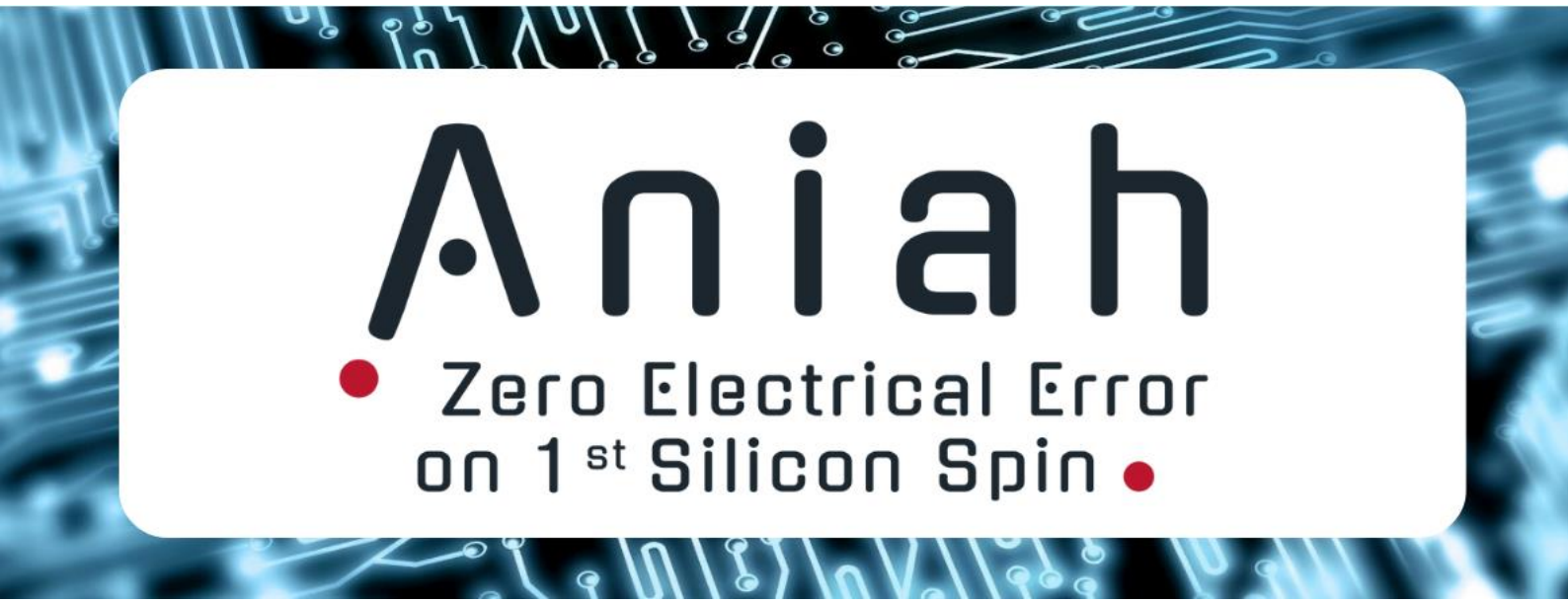


Conditional HiZ: vulnerable circuits, consequences, and failsafe detection techniques

Kenza Ghefir - *Application Engineer* - Aniah

Vincent Bligny – *CEO* - Aniah

Content

1 Introduction

Transistors are highly non-linear devices. Their channel impedance may vary from 10s of Ohms to Giga-Ohm values depending on the bias applied on their terminals. It may occur that, under certain conditions, some circuit nets may become “loose” because they are connected only to high-impedance devices. Circuit designers customarily check their designs for occurrence conditions of High Impedance Nets (HiZ nets). However, some complex cases with multi-stable states may escape their vigilance. Besides, the condition may depend on system-level power-down signaling and thus requires a full-chip design review.

Conditional High-Impedance nets are hard-to-predict and their consequences are usually even harder to detect, often non-systematic. HiZ nets may create a wide range of issues throughout the Validation, Qualification and Ramp-up of an IC design:

- **Power consumption** - Floating nodes can constantly charge and discharge parasitic capacitances, leading to higher standby current.
- **Reliability** – HiZ nets will settle over time on a voltage that depends on transistors Roff and may exceed the maximum rating of devices. The reliability risk is heightened by its strong dependency with temperature, corner and ageing.
- **Timing violations** - Signals passing through logic with a floating node input may experience variations in propagation delay. This can disrupt the timings.
- **Latch-up** - Floating nodes can increase the risk of latch-up through high impedance cross-talk between two nodes, allowing the parasitic thyristor to trigger.
- **ESD** - Floating nodes can increase the risk of ESD by creating a charge buildup in the IC, which can discharge suddenly and cause damage.[1]
- **Crosstalk** - Noisy floating nodes can couple their signal onto nearby interconnects, interfering with other nodes through capacitive and inductive crosstalk.[2]

Conditional HiZ nets create a range of issues during an IC design project – and are among the errors most likely to be detected late during a project. Consequences range from re-spin of the design, failed time-to-market, market loss, and product recalls. The severity of Conditional HiZ errors is further strengthened by the potentially non-systematic nature of those errors.[3]

The figure (1) shows the impact of project delays on revenue (here neglecting Silicond lead-time).

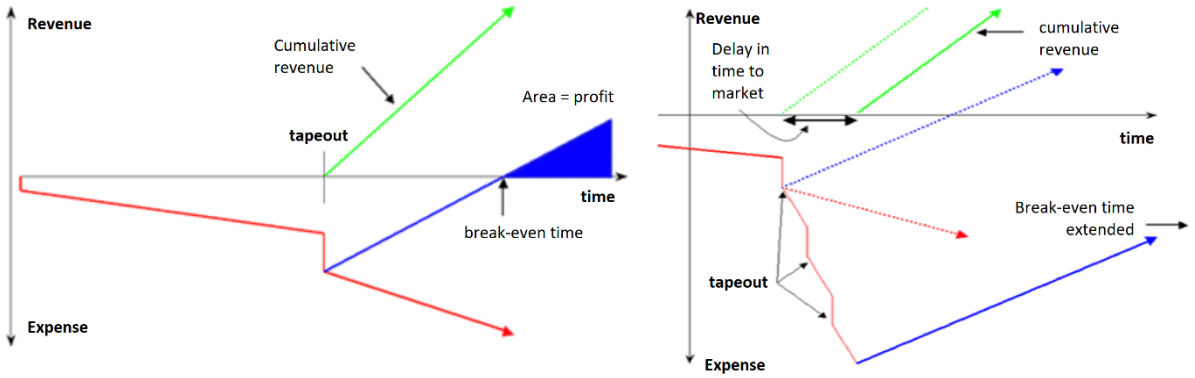
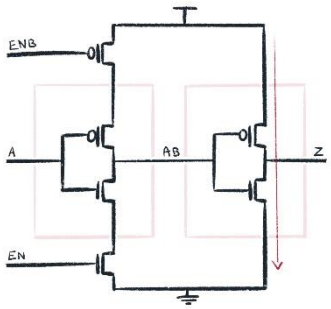


Figure 1 : Idealized revenue growth and profit for an IC achieving first-silicon success and immediate volume sales versus Impact of silicon re-spins on time-to-market and time-to-profit. [3]

Because of design complexity and gaps in verification capabilities, the semiconductor industry, on average, needs two or more silicon re-spins for over 50% of advanced designs.[3]

When manufacturing semiconductor devices, consistent quality and reliability must be built into them from the development to the manufacturing stage to prevent defects in the field. **Aniah OneCheck** is an advanced circuit verification tool that ensures the robustness of a design by formally proving the compliance with advanced electrical rules that define IC performance standards and reduce premature or catastrophic electrical failures.

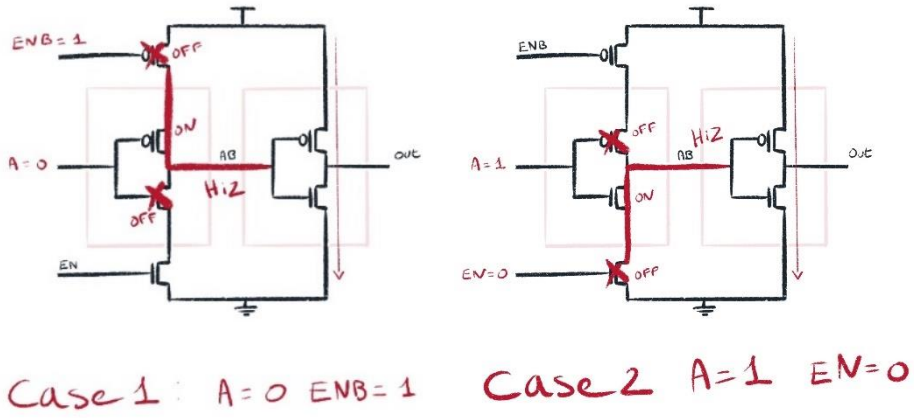
2 Case study 1: HiZ condition on a purely combinatorial case



The simplest case of Conditional HiZ is purely combinatorial conditions: the error is systematic and doesn't depend on the previous states of the circuit.

On this example, 4 conditions on input signals may result in AB being HiZ, and a subsequent current leakage in the output inverter:

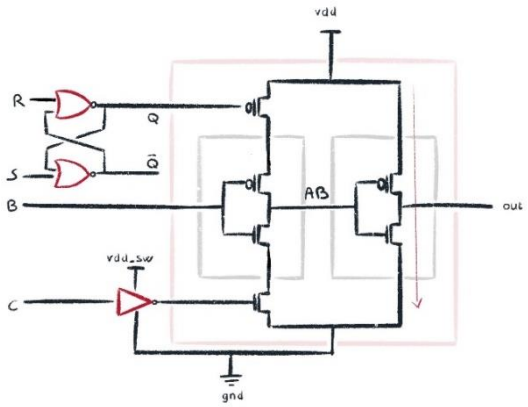
ENB	EN	A	AB
0	0	0	1
0	0	1	HiZ
0	1	0	1
0	1	1	0
1	0	0	HiZ
1	0	1	HiZ
1	1	0	HiZ
1	1	1	0



3 Case study 2: HiZ condition on retained states – flips-flops

When the design includes flip-flops, the detection of Conditional HiZ nets becomes more complex, as they depend not only on the current state, but also on the values retained.

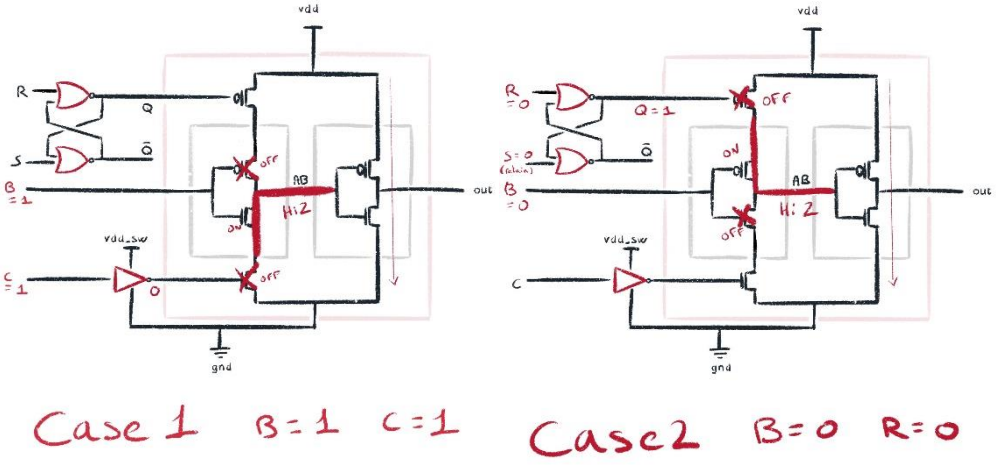
This configuration is particularly dangerous as simulation-based techniques may fail to detect it if the testbench doesn't include the relevant scenario – in other words, the stimuli must, in a way, "know about the error case" to ensure full coverage.



In addition, in the case shown here, a signal is driven by a switched power supply. Consequently, errors conditions will depend on whether the supply is turned off.

An exhaustive list of error conditions is provided:

B	C	R	S	Q	vdd_sw	AB
0	1 or 0	0	0	1	1	HiZ
0	1 or 0	0	1	1	1	HiZ
1	1	1 or 0	1 or 0	1 or 0	1	HiZ
1	1 or 0	1 or 0	1 or 0	1 or 0	0	HiZ

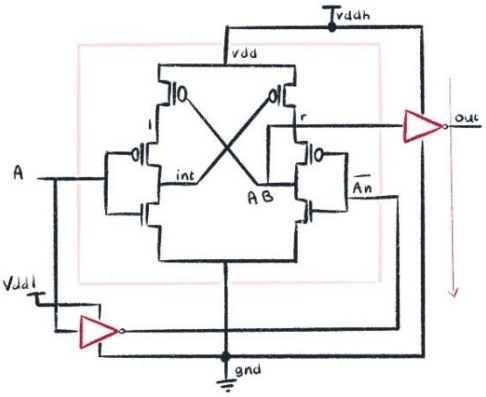


An interesting case is R=S=B=0. In this case, the occurrence of the error depends on the value of Q, which may be 0 or 1 depending on the previous states of the circuit, this is called a latch.

4 Case study 3: HiZ in non-CMOS circuitry

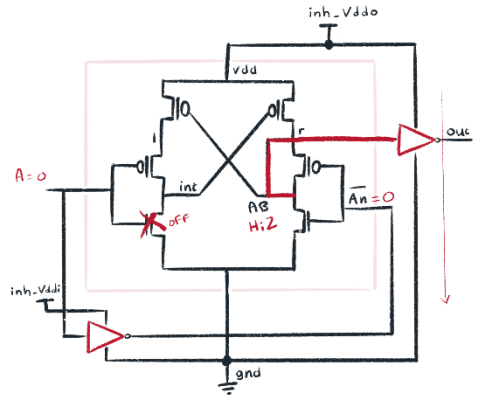
Conditional HiZ errors may also occur in non-CMOS circuitry – which may be analog circuitry or, as in the example below, a level shifter.

HiZ errors detection on non-CMOS circuitry requires to consider analog values for all nets. In the circuit below with a feedback loop, AB=HiZ means that 'int' will be pulled to 'vdd' and hence, AB will be left HiZ : this is a stable state.



This type of errors is particularly difficult to detect with Spice simulation as the simulator may not converge on the state in error.

This circuit has only 1 input ‘A’. However, the state of the input-stage supply ‘vddl’ must be considered as A=An=0 when vddl is ‘off’.



A	vddl	AB	Out
0	0	HiZ	X
0	1	0	1
1	0	1	0
1	1	0	0

5 Aniah OneCheck HiZ : detection conditional HiZ errors with full coverage

Aniah has developed a novel solution to detect HiZ errors with 4 foundational objectives:

- The detection must run at IC scale, up to billions of transistors, as some failure conditions are due to system-level connectivity.
- Errors in analog circuitry must be detected, with a maximum transistor count in a topology over a thousand.
- Intentional and non-intentional memories (bi-stable nets) must be identified to detect error conditions depending on signals history.
- The solution must run “out-of-the-box” on process nodes from BCD-130nm to cutting edge N3.

Those 4 points are required to achieve a 100% coverage of conditional HiZ nets.

Aniah OneCheck HiZ has been benchmarked on a variety of designs:

Process node	Transistor count	Errors (digital + iso)	Errors (analog)	Runtime
BCD 130nm	400k	220	8	2 min.
Sensor 40nm	200M	2400	4	5 min.
Finfet 16nm	6B	8	1	12 min.
N3 (MS IP)	45M	530	135	8 min.

This benchmark demonstrates the capacity of Aniah OneCheck HiZ to run on all types of circuitry, at all scales, on the full range of process nodes. It has shown both the robustness of Aniah OneCheck HiZ – 100% of errors were found – but also the complete absence of false errors.

6 Conclusion

Conditional HiZ errors are among the most serious risks in an IC project because of their capacity to elude Silicon qualification phases and escape into mass-production.

Considering the low resource investment needed to achieve a 100% detection of such errors before taping-out with Aniah OneCheck HiZ, the deployment of a solution to detect HiZ nets is strongly advised as an IC verification step with an unparalleled cost-benefit-ratio.

The Conditional HiZ detection tools, that conclude with “forbidden states” at IP level without the need for a simulation testbench, are ideally suitable for a bottom-up, early verification flow, while the “check-and-save class” runtime of Aniah OneCheck HiZ, through immediate detection, further reduces the cost to fix errors.

References

1. "CMOS Circuit Design, Layout, and Simulation" by R. Jacob Baker, Harry W. Li, and David E. Boyce.link[1]
2. "Analysis and Design of Analog Integrated Circuits" by Paul R. Gray and Robert G. Meyer.link[2]
3. "The Risk/Reward Realities of Chip Development" by Simon Young.link[3]
4. "Digital Integrated Circuit Design" by Ken Martin.link[4]

Contact us for more information :

Mail : contact@aniah.fr

Website : www.aniah.fr

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